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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,317	02/07/2002	Joseph W. Ku	10013828-1	7043

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/067,317	KU ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the election on 22 December 2004. Claims 1-20 are pending.

Election/Restrictions

The restriction requirement made in the Office action mailed on 3 December 2004 is hereby withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Grzyb et al. (5,656,834).

Referring to claim 1, Grzyb et al. disclose a method of forming an integrated circuit where a circuit function block is formed on an IC chip; and forming a decoupling capacitor (20) in an area above the circuit function block (col. 3, line 65 thru col. 4, line 3).

Claims 16 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Appel (6,653,681).

Referring to claim 16, Appel discloses an integrated circuit where a circuit function block has a predetermined circuit layout; and an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block (col. 1, lines 31-37).

Referring to claim 20, Appel discloses the inter-digitated metal fingers extending from the metal plate in such a manner that the plurality of inter-digitated metal fingers are in parallel and have a predetermined separation and width (Fig. 1; col. 2, lines 20-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 6-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grzyb et al. in view of Appel (6,653,681).

Grzyb et al. disclose the subject matter claimed above except forming a top metal layer; forming a bottom metal layer; and forming an inter-digitated capacitance structure between the top metal layer and bottom metal layer, wherein the inter-digitated

capacitance structure is operated on to generate a predetermined pattern of inter-digitated metal fingers.

Referring to claims 2 and 11, Appel discloses an integrated circuit where a circuit function block has a predetermined circuit layout; and an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block. Appel further discloses forming a top metal layer; forming a bottom metal layer; and forming an inter-digitated capacitance structure between the top metal layer and bottom metal layer, wherein the inter-digitated capacitance structure is operated on to generate a predetermined pattern of inter-digitated metal fingers an integrated circuit where a circuit function block has a predetermined circuit layout; and an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block (Fig. 1; col. 1, lines 31-37).

Since Grzyb et al. and Appel are both from the same field of endeavor, an integrated circuit, the purpose disclosed by Appel would have been recognized in the pertinent art of Grzyb et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Grzyb et al. by forming a top metal layer; forming a bottom metal layer; and forming an inter-digitated capacitance structure between the top metal layer and bottom metal layer, wherein the inter-digitated capacitance structure is operated on to generate a predetermined pattern of inter-digitated metal fingers as taught by Appel to improve the capacitance (col. 1, lines 40-56).

Referring to claims 3 and 12, Appel discloses forming an at least one inter-digitated metal; forming a plurality of inter-digitated metal fingers extending outward from the at least one inter-digitated metal; and forming dielectric material, which is deposited between the at least one inter-digitated metal fingers (Fig. 1; col. 1, lines 31-36; col. 2, lines 20-25).

Referring to claims 4 and 9, Grzyb et al. disclose forming a dielectric layer (37) below the inter-digitated metal fingers and the bottom metal layer (40), wherein the first dielectric layer (37) has a predetermined thickness (Fig. 3 & 5; col. 4, lines 18-29).

Referring to claims 6, 13, 15 and 19, Grzyb et al. disclose forming a dielectric layer (42) above the circuit block and between the inter-digitated metal fingers and the top metal layer (44) (Fig. 3 & 5; col. 4, lines 29-36).

Referring to claim 7, Grzyb et al. disclose the second dielectric layer comprises a predetermined dielectric material (col. 4, lines 29 and 30).

Referring to claim 8, Grzyb et al. disclose a first metal layer (35) as a plate, which isolates the de-coupling capacitor from the circuit block (col. 13-16).

Referring to claim 10, Grzyb et al. disclose forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer, and the first dielectric layer and second dielectric layer (col. 8, lines 1-31).

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Appel in view of Grzyb et al.

Appeal discloses the subject matter claimed above except a plurality of de-coupling capacitances formed between the inter-digitated capacitance structure and first and second metal layers.

Grzyb et al. disclose a method of forming an integrated circuit where a circuit function block is formed on an IC chip; and forming a decoupling capacitor (20) in an area above the circuit function block (col. 3, line 65 thru col. 4, line 3).

Referring to claim 17, Grzyb et al. disclose de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer (col. 8, lines 1-31).

Since Appel and Grzyb et al. are both from the same field of endeavor, an integrated circuit, the purpose disclosed by Grzyb et al. would have been recognized in the pertinent art of Appel. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Appel by de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer as taught by Grzyb et al. to increase capacitance (abstract).

Referring to claim 18, Grzyb et al. disclose a first dielectric layer (32) formed on the circuit function block; a third dielectric layer (42) formed on the second metal layer (40); and a third metal plate (44) formed on the third dielectric layer (42) (Fig. 3; col. 4, lines 11-25).

Referring to claim 19, Grzyb et al. disclose forming a dielectric layer (42) above the circuit block and between the inter-digitated metal fingers and the top metal layer (44) (Fig. 3 & 5; col. 4, lines 29-36).

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grzyb et al. in view of Appel as applied to claims 1 and 11 above, and further in view of Daubenspeck et al. (6,496,053).

Grzyb et al.1in view of Appel disclose the subject matter claimed above except the first dielectric layer is a low dielectric material.

Daubenspeck et al. disclose an integrated circuit where a circuit function block has a predetermined circuit layout; and an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block (Fig. 14; col. 6, lines 40-44).

Referring to claims 5 and 14, Daubenspeck et al. disclose a first dielectric layer (150) as a low dielectric material (col. 1, lines 31-35).

Since Grzyb et al. and Daubenspeck et al. are both from the same field of endeavor, an integrated circuit, the purpose disclosed by Daubenspeck et al. would have been recognized in the pertinent art of Grzyb et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Grzyb et al. by a first dielectric layer as a low dielectric material as taught by Daubenspeck et al. to increase reliability (col. 1, lines 46-54; col. 7, lines 43-50).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Roche et al. (6,830,650) disclose an inter-digitated capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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